WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a semiconductor substrate;

a memory cell section including a memory cell transistor formed on said semiconductor substrate;

a plate contact section including a plate transistor formed on said semiconductor substrate;

a first interlayer insulation film formed on said semiconductor substrate to cover said memory cell transistor and said plate transistor;

an etch stop layer formed on said first interlayer insulation film;

a ferro-electric capacitor including a lower electrode connected to said memory cell transistor, a ferro-electric film and an upper electrode, and formed on said etch stop layer in said memory cell section;

a second interlayer insulation film formed on an entire surface of said substrate to cover said ferro-electric capacitor;

a first contact hole corresponding to said ferro-electric capacitor and formed in said second interlayer insulation film in said memory cell section to expose said upper electrode of said ferro-electric capacitor;

a second contact hole formed in said second interlayer insulation film in said plate contact section; and

a plate line provided to connect said upper electrode and said plate transistor through said first contact hole and said second contact hole.

2. The semiconductor memory device according to claim 1, further comprising:

a first conductor formed to penetrate said first interlayer insulation film and said etch stop layer, and providing an electrical connection between said lower electrode of said ferro-electric capacitor and said memory cell transistor; and

a second conductor formed to penetrate said first interlayer insulation film and said etch stop layer, and providing an electrical connection between said plate transistor and said plate line formed in said second contact hole.

3. The semiconductor memory device according to claim 1, wherein said etch stop layer is made of a material which is etched at a rate slower than a rate at which said second interlayer insulation film is etched under etch condition used to form said first and second contact holes.

4. The semiconductor memory device according to claim 3, wherein said etch stop layer is made of a material which is etched at a rate slower than a rate at which said first interlayer insulation film is etched under etch conditions used to form said first and second contact holes.

5. The semiconductor memory device according to claim 1, wherein said second interlayer insulation film is being planarized.

6. The semiconductor memory device according to claim 5, further comprising contact studs formed in said first contact hole and said second contact hole.

7. A semiconductor memory device comprising:

a semiconductor substrate;

a memory cell transistor having source and drain regions formed in said semiconductor substrate;

a first interlayer insulation film formed on said semiconductor substrate to cover said memory cell transistor;

an insulating layer formed on said first interlayer insulation film and made of such a material that resists an etchant etching an overlying layer directly covering said insulating layer;

a ferro-electric capacitor including a lower electrode formed on said insulating layer, a ferro-electric film formed on said lower electrode and an upper electrode formed on said ferro-electric film; and

a first contact stud selectively formed in said insulating layer and said first interlayer insulation film to provide a conductive path between one of said source and drain regions of said memory cell transistor and said lower electrode of said ferro-electric capacitor.

8. The semiconductor memory device according to claim 7, further comprising:

a plate transistor having source and drain regions formed

in said semiconductor substrate;

a second interlayer insulation film formed on said insulating layer and provided as said overlying layer to cover said ferro-electric capacitor;

a first contact hole formed in said second interlayer insulation film to expose said upper electrode of said ferro-electric capacitor;

a second contact hole formed in said second interlayer insulation film and located above one of said source and drain regions of said plate transistor;

a second contact stud selectively formed in said insulating layer and said first interlayer insulation film to make electrical connection to one of said source and drain regions of said plate transistor; and

a plate line providing electrical connection between said upper electrode of said ferro-electric capacitor and said second contact stud.

9. The semiconductor memory device according to claim 7, wherein said overlying layer is a second uppermost level of insulating layer underlying an uppermost level of insulating layer.

10. A semiconductor memory device comprising a memory cell transistor having a ferro-electric capacitor, and a plate transistor connected to an upper electrode of said ferro-electric capacitor,

said plate transistor comprising:

source and drain regions selectively formed in a semiconductor substrate;

a first layer insulation film covering said source and drain regions;

an insulating layer formed on said first interlayer insulation film and made of a material different from that making up said first interlayer insulation film;

a contact stud selectively formed in said first interlayer insulation film and said insulting layer to make electrical connection to one of said source and drain regions of said plate transistor;

a second interlayer insulation film formed on said insulating layer; and

a contact hole formed in said second interlayer insulation film to provide electrical connection between said contact stud and said upper electrode of said ferro-electric capacitor.

11. The semiconductor memory device according to claim 10, further comprising a plate line electrically connecting said contact stud and said upper electrode of said ferro-electric capacitor wherein at least a part of said contact stud contacts said plate line through said contact hole and a portion, adjacent said at least a part of said contact stud, of said insulating layer contacts said plate line through said contact hole.

12. The semiconductor memory device according to claim 10, wherein said contact stud entirely contacts said plate line through said contact hole and portions, surrounding said contact

stud, of said insulating layer contact said plate line through said contact hole.

13. The semiconductor memory device according to claim 10, wherein said second interlayer insulation film is a second uppermost level of insulating layer underlying an uppermost level of insulating layer.